Modification of thermal boundary resistance for thermal management of interconnect system in advanced VLSI circuits

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To meet the ever-growing demand for higher performance and complex functionality from computing needs such as wireless communication, cloud computing, and artificial intelligence, the logic technology node of VLSI circuits has shrunk to 5 nm. Meanwhile, the half-pitch dimension of interconnects, as a network for power and clock distribution between components in VLSI, scales accordingly and will reach 8 nm after 2025, as predicted by the International Roadmap for Device and Systems (IRDS). Current flow in interconnects causes temperature increase due to the Joule heating effect. Thermal management of interconnects has become one of the most important factors determining the performance and the reliability of advanced VLSI circuits.[1] Parameters affecting interconnect temperatures, such as interconnect wire resistivity, current density, thermal conductivity of interlayer dielectrics, and via density, etc. have been analysed in previous study.[2] However, thermal boundary resistance (TBR) between interconnect wires and the surrounding dielectrics, has either been ignored or treated approximately, which may cause significant uncertainty of the performance and reliability of VLSI interconnects.[3]

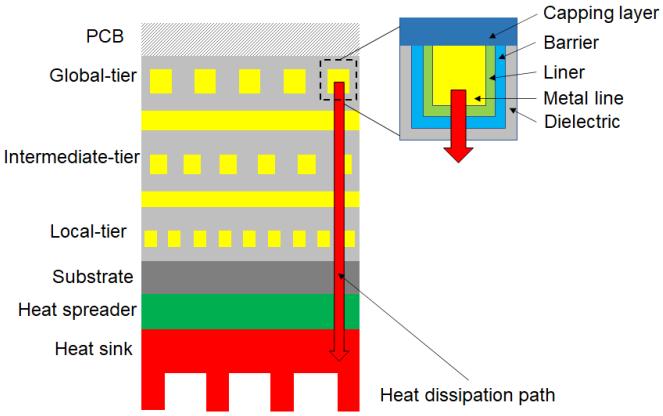

Figure 1. Schematics of heat dissipation path in multilevel interconnect system of VLSI circuits. The inset shows the cross-sectional view of metal/liner/barrier/dielectric interconnect structure.

In this study, metal/interlayer/dielectric film stacks were prepared to mimic the interconnect structure in VLSI circuits. The TBRs of the film stacks were measured by the frequency domain thermoreflectance (FDTR) method. X-ray diffraction (XRD), energy-dispersive X-ray spectroscopy (EDS), and hard X-ray photoelectron spectroscopy (HAXPES) methods were employed to characterize the crystallinity, composition, and chemical bonding of the film stacks. 3D electrothermal finite element method (FEM) was used to simulate the temperature increase in interconnect system. Results indicate that the measured TBR is significantly higher than the values predicted by the diffuse mismatch model (DMM) and varies widely depending on the interlayer used. FEM simulations show that such a high TBR can cause a temperature increase of hundreds of degrees in the advanced VLSI interconnect. Characterizations show the significant importance of interfacial bonding in TBR, which could be modified to decrease the TBR for thermal management of advanced VLSI circuits.

References:

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